A Circuit-Based Approach to Efficient Enumeration

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May 10th, 2017

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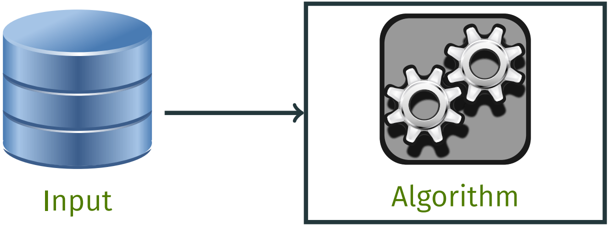
[4]CNRS CRIL

Problem statement

Problem: Enumerating large result sets

Input

Problem: Enumerating large result sets



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a	b	c
a’	b	c
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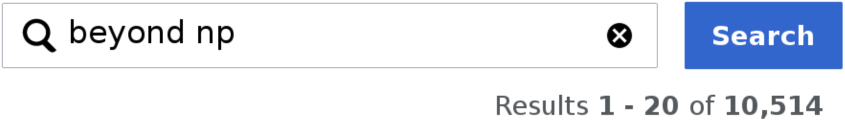

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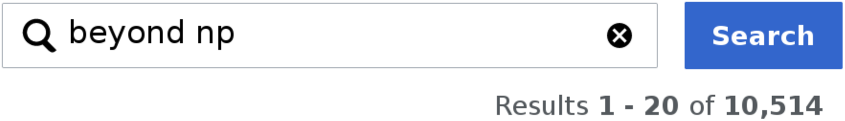

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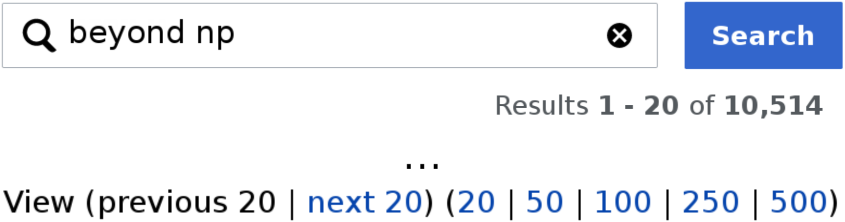

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beyond np

Search

Results **1 - 20** of **10,514**

...

View (previous 20 | next 20) (20 | 50 | 100 | 250 | 500)

→ Solution: Enumerate solutions one after the other

Enumeration algorithm

Input

Enumeration algorithm

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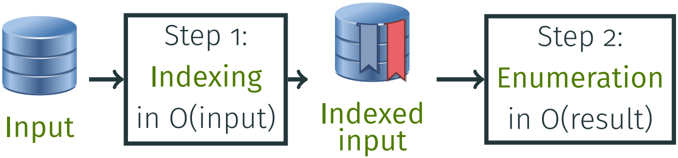

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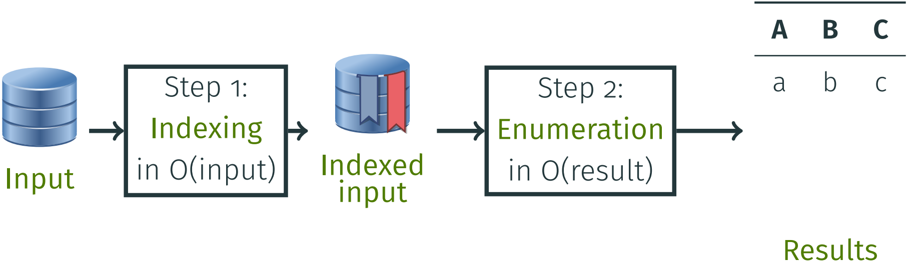

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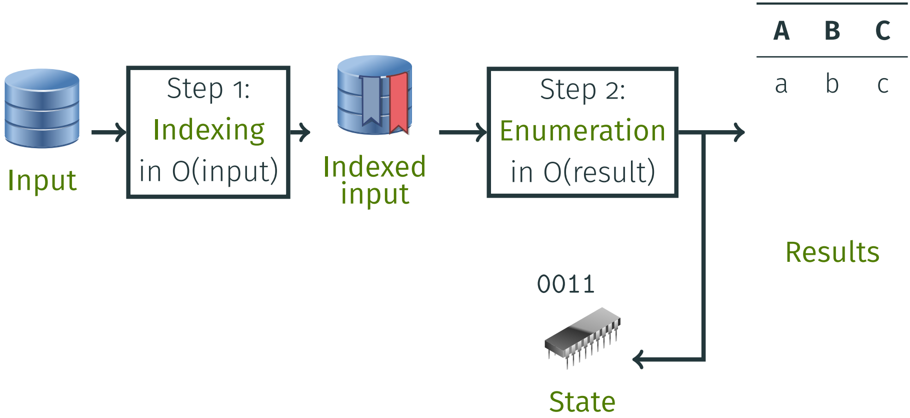

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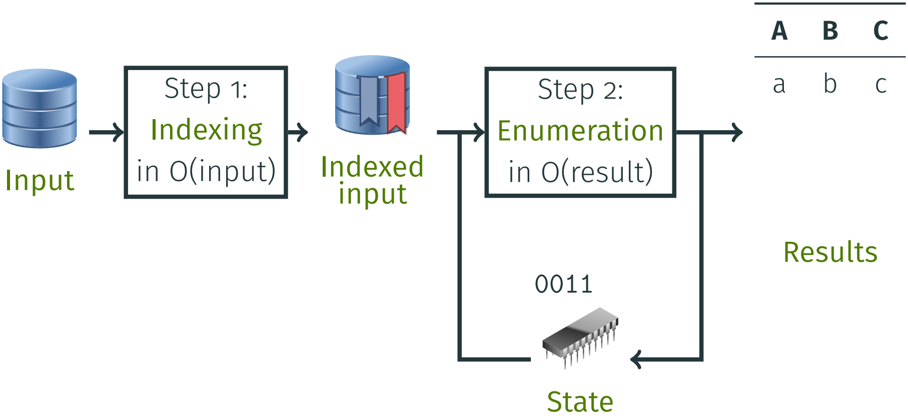

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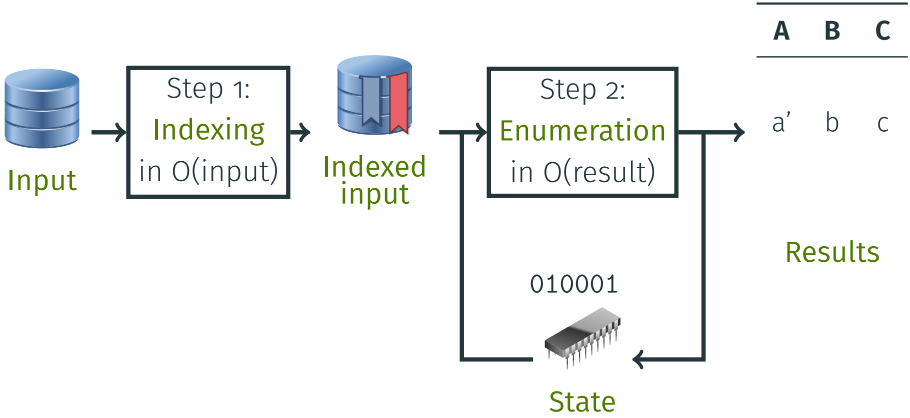

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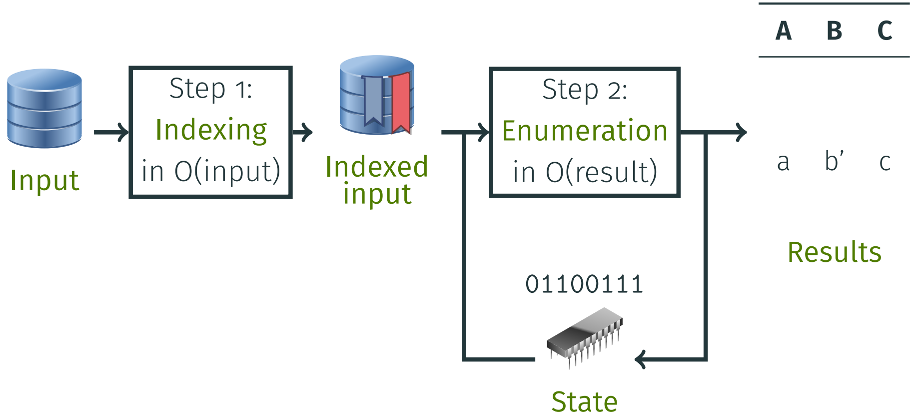

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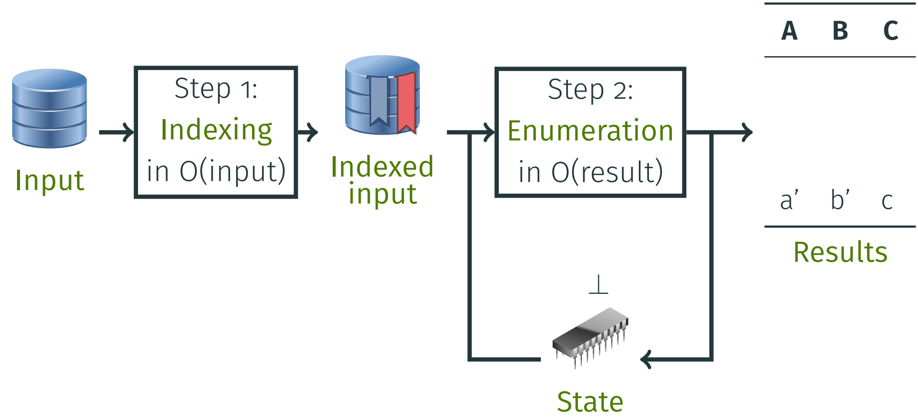

General idea for enumeration

Currently:

Input

Enumeration

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Results

General idea for enumeration

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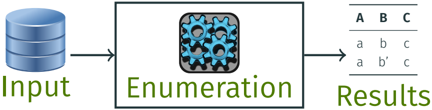

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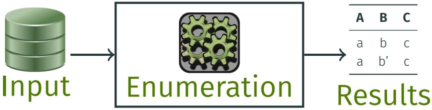

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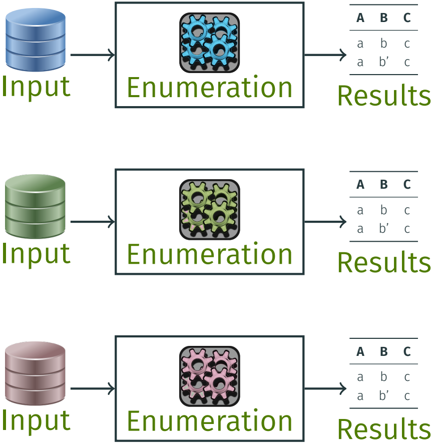

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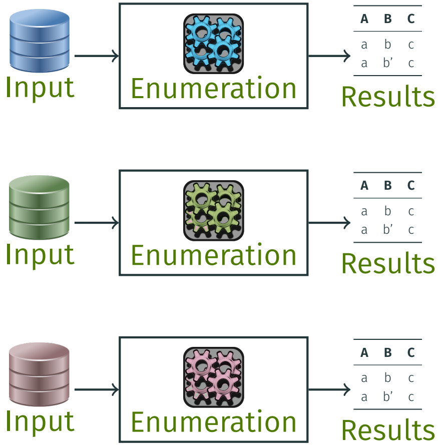

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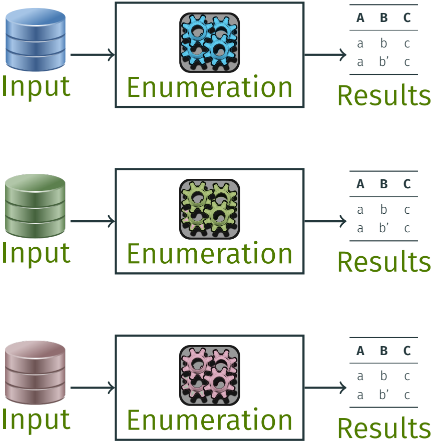

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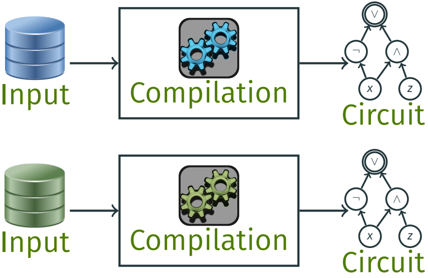

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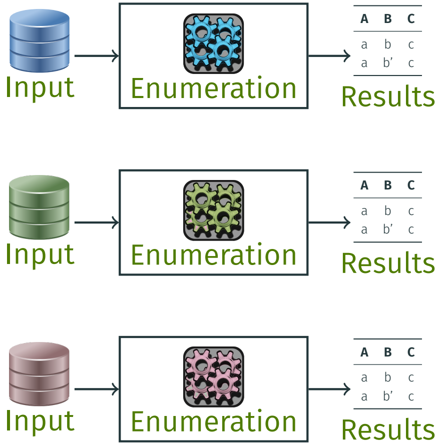

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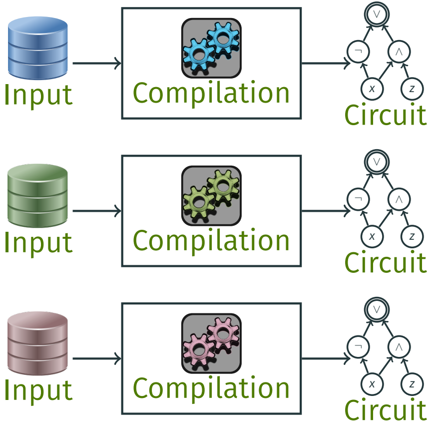

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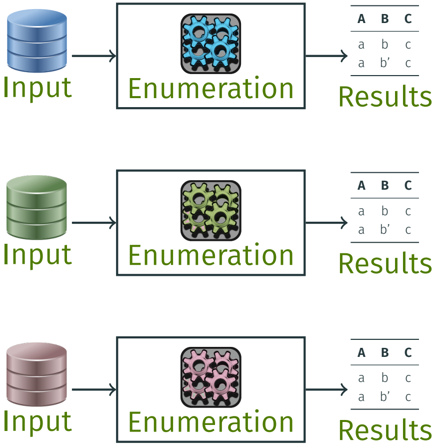

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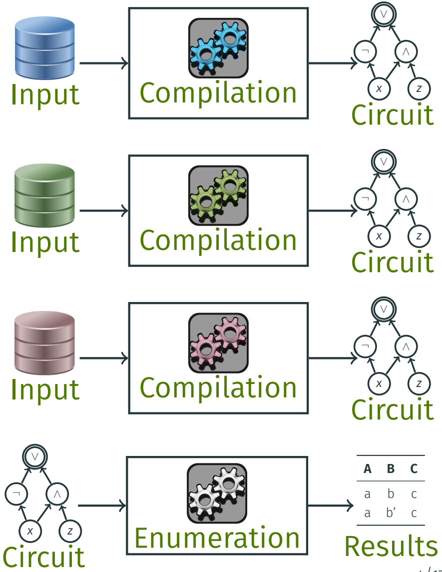
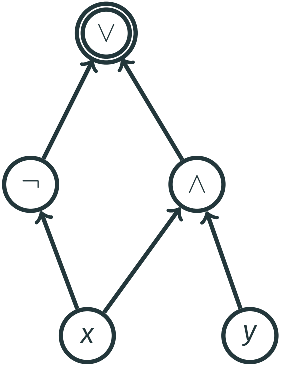


Boolean circuits



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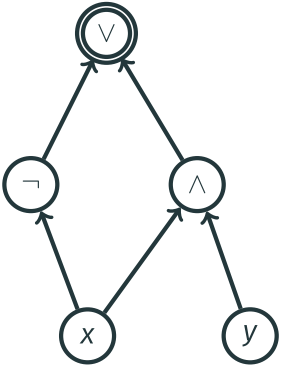
Boolean circuits



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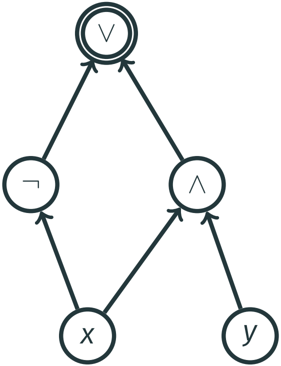

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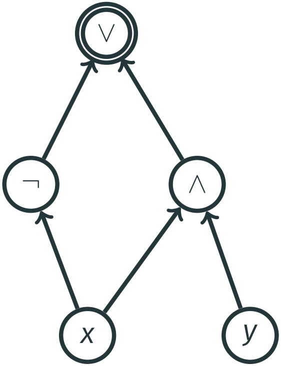
Boolean circuits



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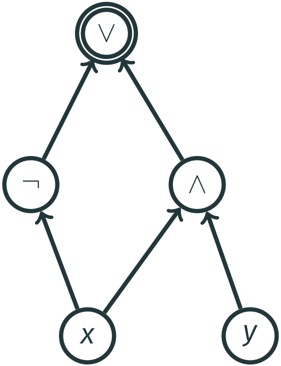

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  Example: $\nu = \{x \mapsto 0,\ y \mapsto 1\}$...

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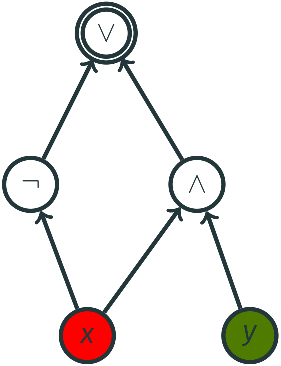

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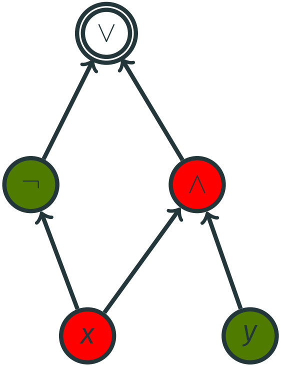

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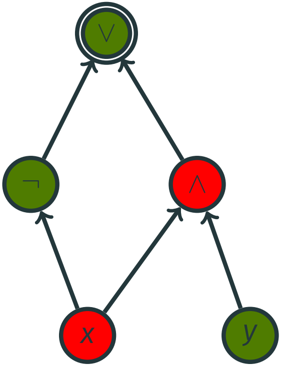

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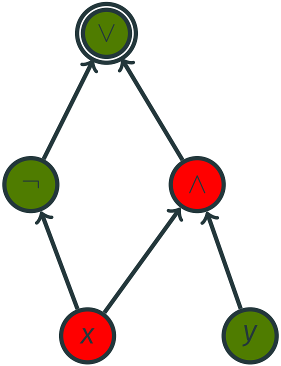

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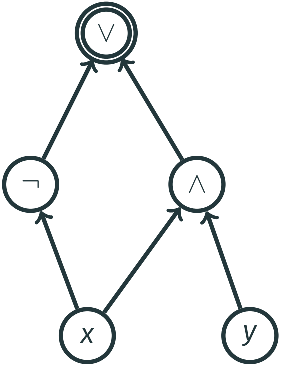

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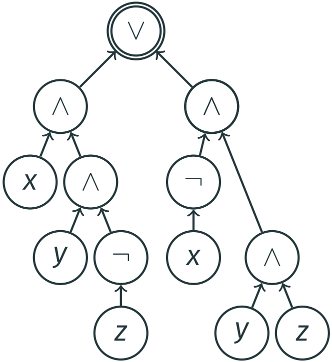
Our task: Enumerate all **satisfying assignments** of an input circuit

Circuit restrictions

d-DNNF:

- $\vee$ are all deterministic:

The inputs are mutually exclusive (= no valuation ν makes two inputs simultaneously evaluate to 1)



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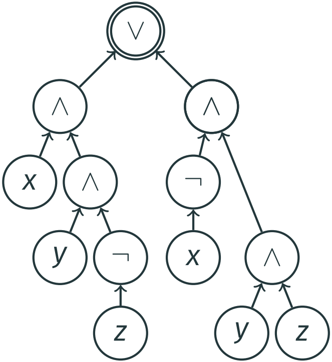

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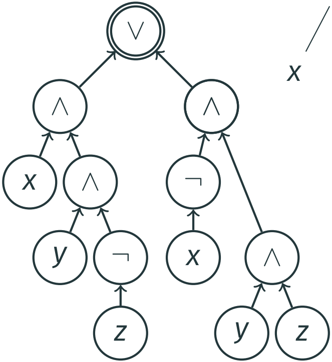
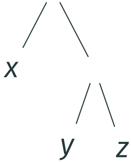
v-tree: $\wedge$-gates follow a tree on the variables





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Also: restrict to assignments of constant size $k \in \mathbb{N}$ (at most k variables are set to 1):

Theorem

Given a d-DNNF circuit C with a v-tree T, we can enumerate its satisfying assignments of size $\leq k$ with preprocessing linear in $|C| + |T|$ and constant delay

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- Factorized databases: implicit representation of database tables

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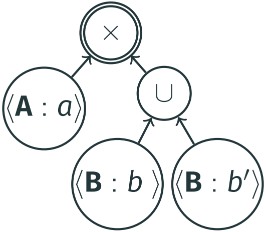

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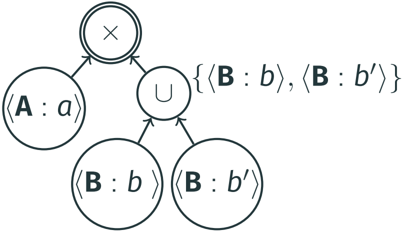

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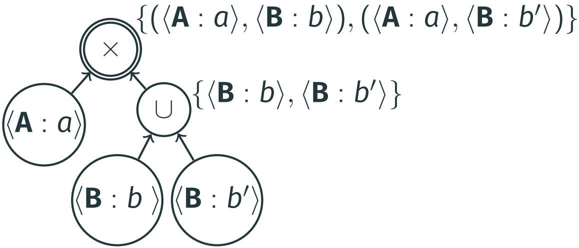

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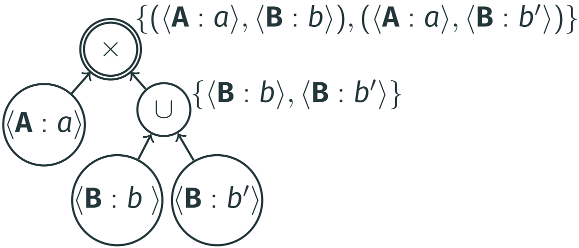

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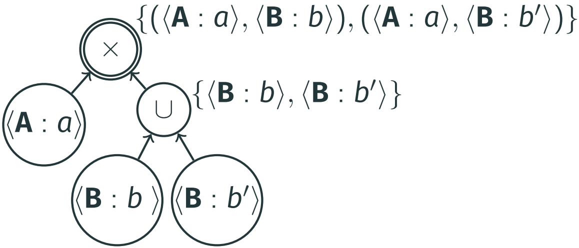

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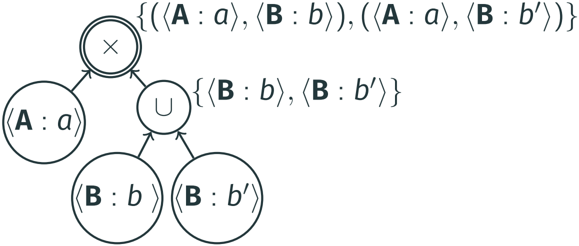

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Theorem (Strenghtens result of [Olteanu and Závodnỳ, 2015])

Given a deterministic factorized representation, we can enumerate its tuples with linear preprocessing and constant delay

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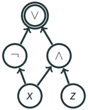
Theorem (Recaptures [Bagan, 2006], [Kazana and Segoufin, 2013])

Given a MSO query Q and a database D, the results of Q on D can be enumerated with linear preprocessing in D and linear delay in each answer ($\rightarrow$ constant delay for free first-order variables)

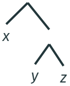
Proof techniques

Proof overview

Preprocessing phase:



Circuit



v-tree

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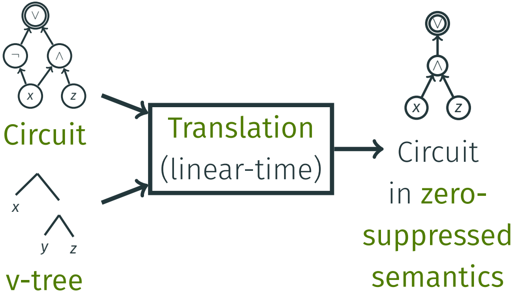

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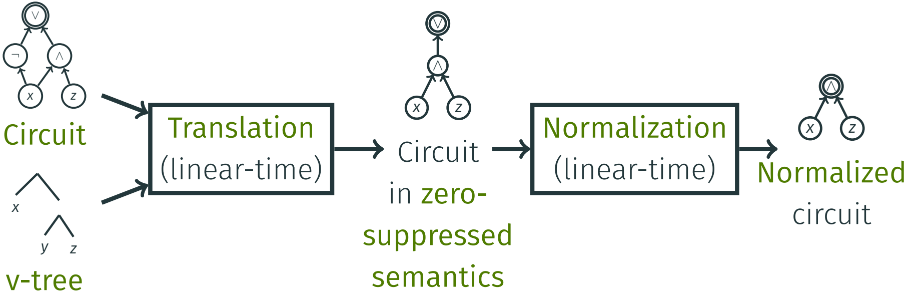

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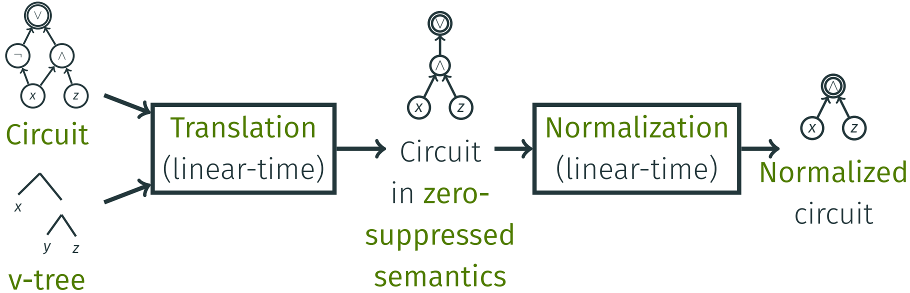
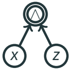


Enumeration phase:



Normalized
circuit

Proof overview

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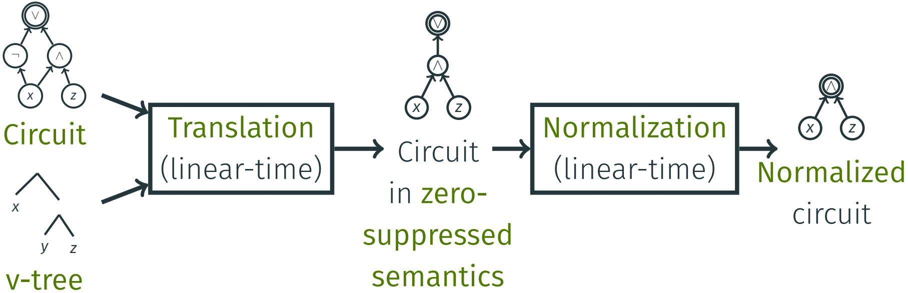

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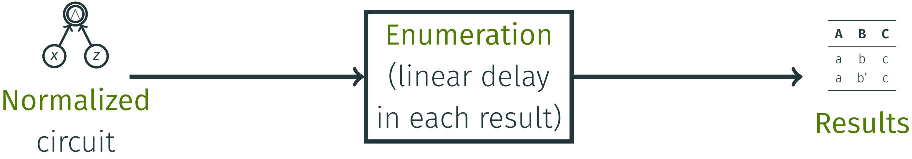
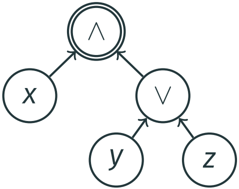


Zero-suppressed semantics



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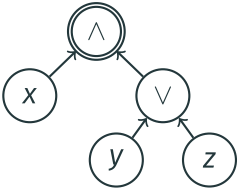

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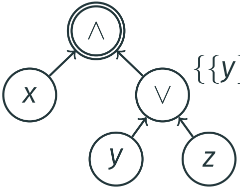

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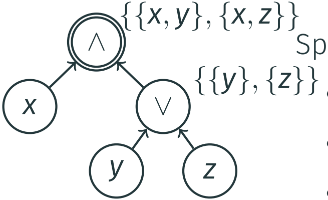

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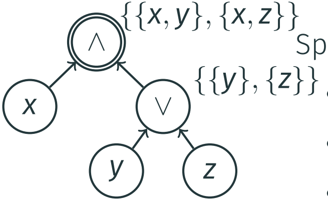

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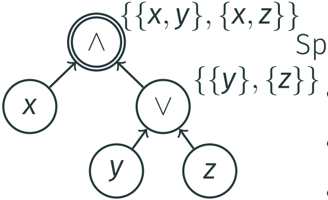

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Many equivalent ways to understand this:

- Generalization of factorized representations
- Analogue of zero-suppressed OBDDs (implicit negation)
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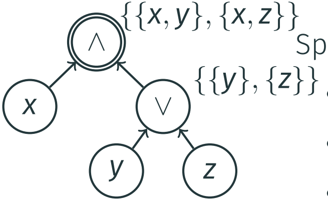

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Simplification: rewrite circuits to arity-two (fan-in ≤ 2)

Enumerating assignments in the zero-suppressed semantics

Task: Enumerate the elements of the set $S(g)$ captured by a gate g

$\rightarrow$ E.g., for $S(g) = \{\{x, y\}, \{x, z\}\}$, enumerate $\{x, y\}$ and then $\{x, z\}$

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OR-gate

$$\begin{tikzcd} & \lor & \\ g \arrow[ur] & & g' \arrow[ul] \end{tikzcd}$$

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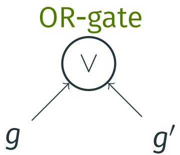

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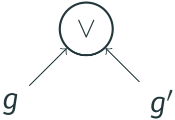

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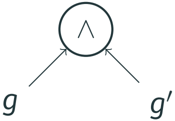
AND-gate



Lexicographic product: enumerate $S(g)$ and for each result t enumerate $S(g')$ and concatenate t with each result

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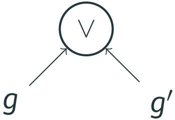

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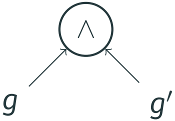

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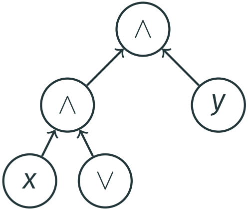
Decomposability: no duplicates

Normalization: handling $\emptyset$



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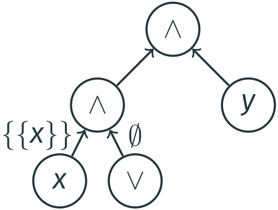

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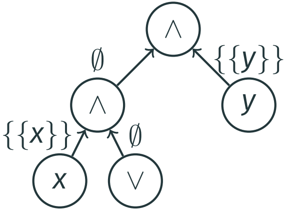

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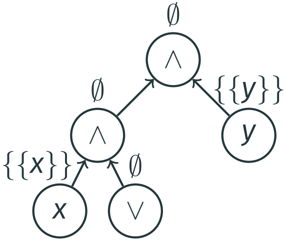

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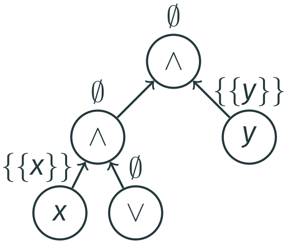

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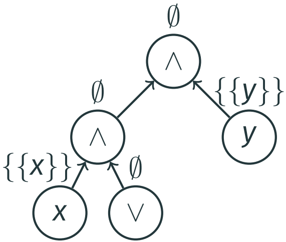

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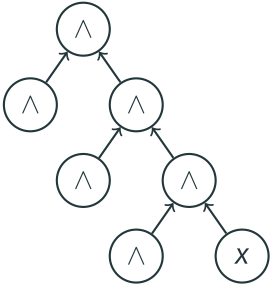
- Solution: compute bottom-up if $S(g) = \emptyset$

Normalization: handling empty assignments



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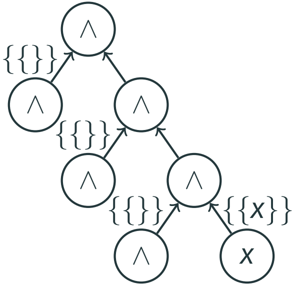

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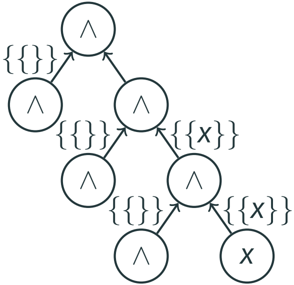

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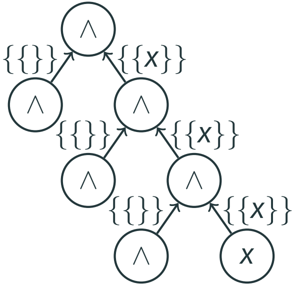

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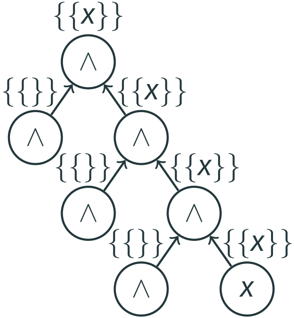

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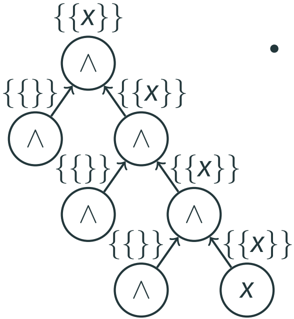

- Problem: if $S(g)$ contains $\{\}$ we waste time in chains of AND-gates

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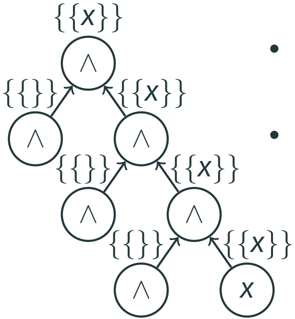

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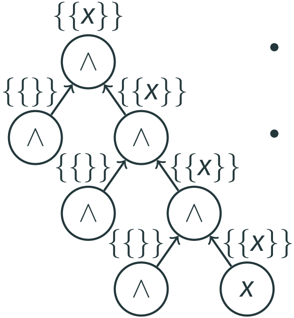

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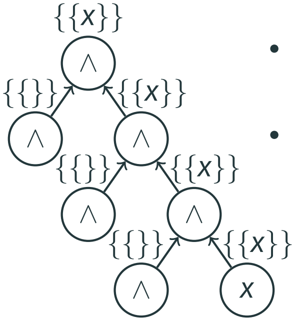

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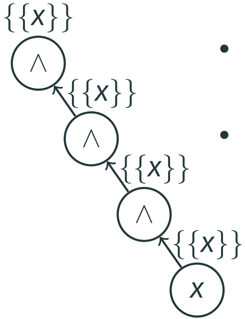

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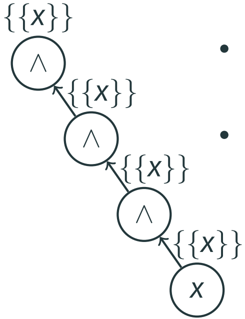

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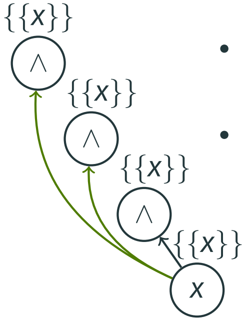

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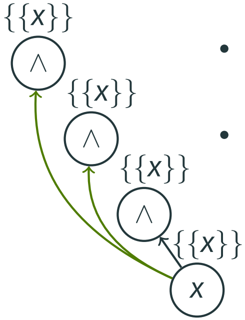

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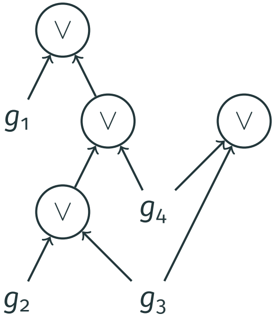
$\rightarrow$ Now, traversing an AND-gate ensures that we make progress: it splits the assignments non-trivially

Normalization: handling OR-hierarchies



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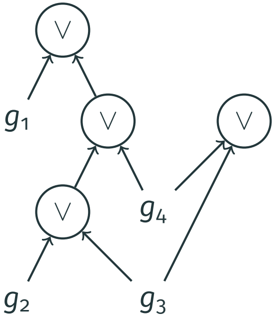

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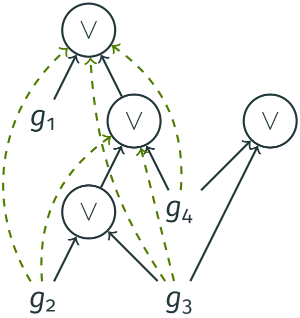

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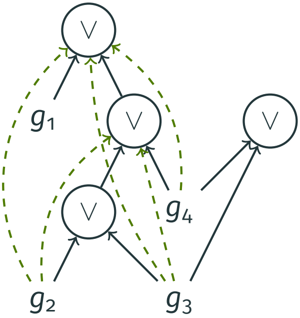

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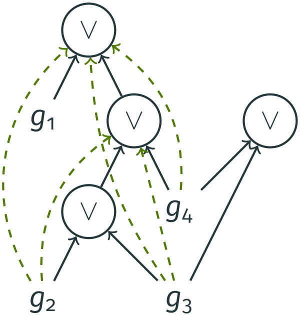

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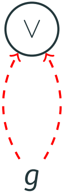
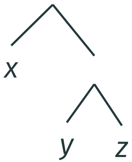
Solution:

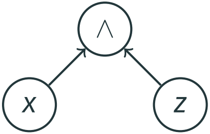
- **Determinism** ensures we have a **multitree** (we cannot have the pattern at the right)
- **Custom** constant-delay reachability index for multitrees



Translating to zero-suppressed semantics

- This is where we use the v-tree





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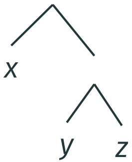
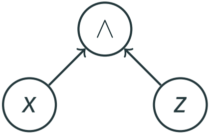
- Add explicitly **untested variables**





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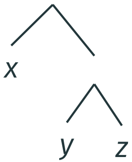

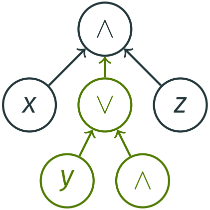

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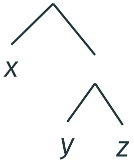

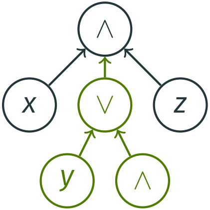

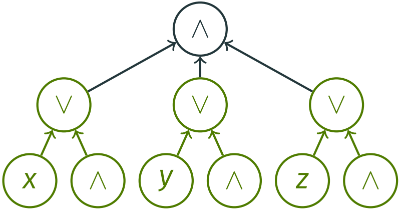

- **Problem:** quadratic blowup

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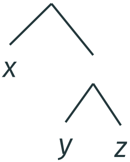

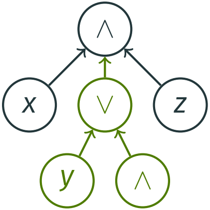

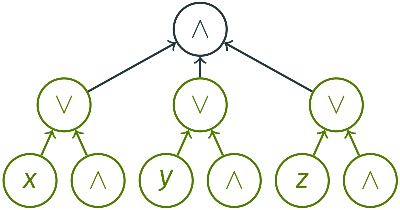

- **Problem:** quadratic blowup
- **Solution:**
  - **Order** $<$ on variables in the v-tree ($x < y < z$)
  - **Interval** $[x, z]$
  - **Range gates** to denote $\bigvee[x, z]$ in constant space

Conclusion

Summary and conclusion

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- Usual approach: develop enumeration algorithms by hand

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  - Develop general enumeration results on circuits

Future work:

- Theory: handle updates on the input
- Practice: implement the technique with automata

Summary and conclusion

Summary:

- Usual approach: develop enumeration algorithms by hand
- Proposed approach:
  - Develop linear-time compilation algorithm to circuits
  - Use restricted circuit classes (structured d-DNNF)
  - Develop general enumeration results on circuits

Future work:

- Theory: handle updates on the input
- Practice: implement the technique with automata

Thanks for your attention!

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